

Optimizing Mixed Alloy Solder Pastes for Low Voiding and High PCB Reliability

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ABSTRACT

High-reliability solders may contain multiple elements (up to 6 or 7 elements) for strength, including intermetallic compound (IMC) particles, precipitates, solid solutions, and fine grains. The complicated alloy composition and microstructure impact solder melting behavior and thus influences the joint voiding performance. Solder joint voids may present a significant reliability challenge in electronics manufacturing, as they can compromise the mechanical integrity of solder joints, inhibit thermal dissipation, and interfere with electrical signal transmission. These effects can downgrade the solder joint performance and lifespan of printed circuit board assemblies (PCBAs), particularly in high-reliability applications. To address these concerns, a novel mixed-alloy solder paste system has been developed to deliver both low voiding and enhanced thermal cycling reliability of the formed solder joints. This system incorporates low-voiding alloy powders that promote early wetting during reflow, while another alloy powder contributes to improving joint strength and durability through reflow. The resulting solder joints are homogeneous. The mixed solder powder paste is designed as a drop-in replacement, requiring no modification to existing SMT reflow profiles.

This work builds on a previous study aimed at reducing voiding in mixed alloy solder systems[1]. By further optimizing the reflow thermal profile, the project evaluated soldering performance on both organic solderability preservative (OSP) and immersion tin (ImSn) surface finishes using updated reflow profiles. Voiding levels were benchmarked against a standard SAC305 solder paste. The improved mixed alloy system consistently achieved voiding rates below 15%, outperforming SAC305.

These results suggest that the optimized solder paste and process can reduce voiding to levels low enough to potentially eliminate the need for vacuum reflow in certain applications.

Key words: DFHR, high-reliability, lead-free, low void, solder.

INTRODUCTION

Solder joint voiding remains a critical reliability concern in electronic packaging, particularly for high-performance and safety-critical applications such as automotive electronics. Excessive voiding can adversely affect both thermal

conductivity and mechanical strength, leading to elevated junction temperatures, accelerated fatigue failure under thermal cycling, and ultimately reduce product lifetime. To address these concerns, industry standards such as IPC-7095 provide general acceptance criteria for voiding in ball grid array (BGA) packages. For bottom-terminated components (BTCs), including quad flat-pack no-leads (QFNs), IPC-A-610, and J-STD-001 are typically applied. The DKE automotive addendum from the IPC-A-610H and J-STD-001H further harmonizes evaluation methods by establishing consistent definitions and standardized procedures for void area measurement, enabling comparability of results across laboratories and studies.

Multiple factors contribute to void formation during the surface mount assembly process, including stencil thickness, reflow profile, and solder paste formulation. While prior studies have explored these factors, they were often examined in isolation, making it difficult to determine their relative importance or understand the interactions between material and process parameters under realistic production conditions. As a result, manufacturers frequently lack a clear hierarchy of process levers for effectively minimizing voiding and improving long-term reliability.

In this study, solder joint voiding was evaluated in accordance with the DKE automotive addendum to ensure standardized measurement practices. A total of 576 data points were collected across a comprehensive matrix of material and process combinations. The key factors investigated included surface finish (OSP vs. ImSn), nano-coated stencil thickness (4 mil vs. 5 mil), reflow profile (Profile A vs. Profile B), and solder paste. Both overall void percentage and maximum individual void size were used as response variables. Since surface finish data was not collected for both stencil thickness levels, this factor was excluded from the analysis. As a result, the interactions were refined to focus only on the remaining variables.

Statistical modeling and effect summary analysis were performed using JMP® software to identify the dominant factors and interactions that influence voiding behavior, with a particular focus on three-way interactions, such as Stencil Thickness × Profile × Solder Paste. X-ray images were examined to assess whether variations in the reflow profiles affected the morphology of the voids.

The objective of this work is to provide a clear, data-driven ranking of factor importance for voiding control in QFN assemblies. This study combines statistical significance, standardized void measurement practices, and physical validation. Together, these methods provide manufacturers with practical guidance on which material and process factors to prioritize. The goal is to reduce voiding, improve assembly reliability, and support robust electronics production for demanding automotive environments.

In light of voiding concerns, attempts have been implemented to determine if the newly developed mixed alloy solder paste (DFHR: SnAgCuBiSbInNi) could deliver voiding performance comparable to, or even lower than, SAC305, the most commonly used lead-free solder[1-2, 4-8].

The experimental methodology followed that of a previous study, with modifications introduced to assess the potential impact of these changes on voiding[1].

Solder Pastes

The solder pastes selected in the current experiment are shown in Table 1. SAC305, Flux A, type 4, 88.5 wt.% solder paste (Paste 1) was used as a control to compare to the selected high-reliability (hi-rel) paste, and DFHR + Flux B, Type 4, 89.0 wt.% solder paste (Paste 2).

Two halogen-free flux formulations were evaluated in this study. Flux A is a robust formulation designed to enhance stencil transfer efficiency, minimize voiding, and extend stencil life. Flux B is optimized for reduced voiding while maintaining excellent printability and formulation stability. Halogen-free fluxes are the industry's preferred path forward for meeting modern environmental, safety, and reliability requirements especially in high-reliability or no-clean applications. Halogen-containing fluxes are still used in legacy or specialty cases but carry trade-offs in regulatory exposure.

Table 1. Solder Paste

Paste 1	SAC305, Flux A, Type 4, 88.5 wt.%.
Paste 2	DFHR, Flux B, Type 4, 89.0 wt.%

Testing Vehicles

The printed wiring board (PWB) is a well-known design that has been used to evaluate solder paste for decades, as shown in Figure 2. It was designed to evaluate bridging, wetting, solder balling, voiding, and graping. The QFN68 pads in this PCB board were used to evaluate the voiding in this experiment, marked by the red circle.

Table 2 lists the details of the PWB. A Cu-OSP and ImSn surface finish were used for testing. QFN68 was made of dummy components with daisy-chained, 68 perimeter leads on 0.5 mm pitch, 10 x 10 mm² body size, 8 x 8 mm² thermal pad, and matte Sn finish, as referenced in Table 2. There were four QFN pads per board with three boards per panel.

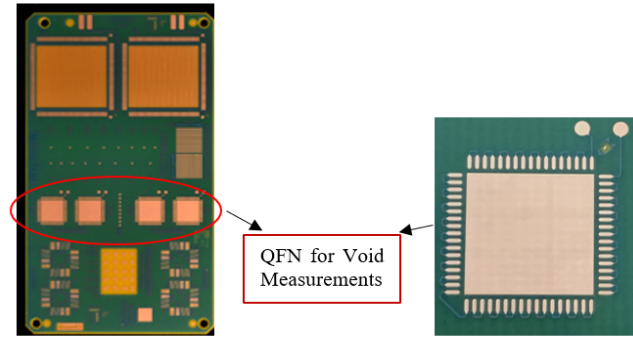


Figure 2. A Bare OSP Test Vehicle PCB QFN Test Board

Table 2. Testing Vehicle

PWB	QFN Test Board	
	Surface Finish	OSP vs. Im-Sn (0.5 oz Cu)
	Tg	170
	Cu-layers	2
Component	Daisy-Chained QFN68	
	Package Size	10 mm x 10 mm
	Thermal Pad size	8 mm x 8 mm
	Metallization	Matte Sn
	Lead Count	68
	Pitch	0.5 mm

Stencil Design

The two test vehicles used stencils with different thicknesses. Even small changes in stencil thickness can significantly affect solder volume, despite an identical nine-pane window design. This is because stencil thickness directly influences paste transfer efficiency and the effective aperture area ratio, which in turn alters the deposited solder volume and coverage.

Both stainless steel stencils had a laser-cut, nano-coated surface and featured the same nine-pane window design, as shown in Figure 3. Each pane consisted of a 2.24 mm (88 mil) square aperture spaced 0.50 mm (20 mil) apart, resulting in a center-to-center pitch of 2.74 mm (108 mil). The full window array measured 7.72 mm (304 mil) across. In both cases, the total stencil aperture-to-pad area ratio was 75%.

The first stencil was 4 mils (0.102 mm) thick and had an area ratio of 5.5 per aperture. The paste volume was 0.51 mm³ per pane, for a total of 4.59 mm³ across the array.

The second stencil was 5 mils (0.127 mm) thick. This reduced the area ratio to 4.4 but increased the paste volume to 0.64 mm³ per pane, totaling 5.76 mm³ for the array.

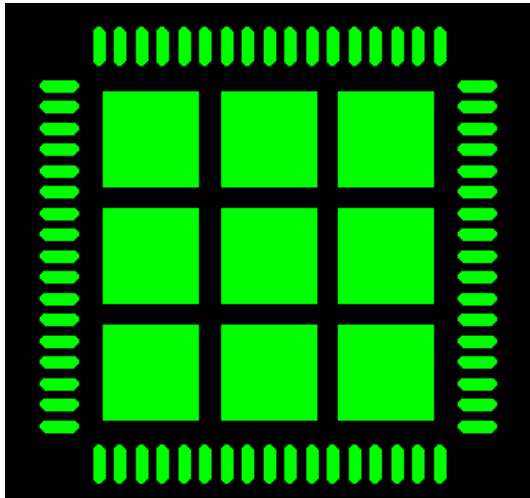


Figure 3. QFN68 Thermal Pad Stencil Design with Standard Cross Hatch

Reflow

An eight-zone convection oven was used for the reflow process. In the previous study, six profiles were tested to observe void formation[1]. In this investigation, two additional profiles were introduced to optimize key reflow parameters such as soaking time, peak temperature, time above liquidus, and heating ramp rate. These profiles were modified based on the reference profile P4 in the previous study. The primary difference between the two new profiles was the ramp rate between 180°C and 220°C, set at 1.0°C/s and 1.5°C/s, respectively. Table 3 summarizes these profiles, while the corresponding reflow profile graphs are provided in the appendix.

For temperature measurement, one thermocouple was placed under each QFN location (QFN 1, QFN 5, QFN 8, and QFN 12) to ensure accurate readings of the test vehicle PCB. An additional thermocouple was used to monitor air temperature, resulting in a total of five thermocouples. Table 3 reports the average temperature readings from all thermocouples for each profile.

Table 3. Profile Breakdown

Profile #	P4	A	B
Peak Temperature (Average in °C)	251	245	245
Time Above Liquidus (Average in seconds)	52	76	0
Slope Between (180-220°C) Ramp Rate (Average in °C/s)	0.64	1.00	1.50
Total Time of Profile (Average in minutes)	4.1	4.00	4.47
Total Time Profile Ramp Rate (Average in °C/s)	0.90	0.90	0.83

EXPERIMENTAL PROCEDURE

Both solder pastes were printed on the PWBs at a speed of 50 mm/s using a print pressure of 5 kg. The stencil separation

distance was 2 mm at a speed of 5 mm/s. Print pressure was optimized by printing four set-up boards. Any printing defects were observed and documented. The stencil was cleaned with a wet/dry/vacuum cleaning profile after each board was printed. The PWBs were processed through pick-and-place and then reflowed. Each board was inspected for voids using DAGE Quadra 7 X-ray inspection. The voiding data was then analyzed with JMP® statistical software. The process is summarized in Table 4.

Table 4. SMT Process

Printer Specifications	MPM Momentum Elite Printer	
	4 mil and 5 mil Nano Laser-Cut Stencil	
	Stainless Steel Squeegee Blades at 60°	
Print Parameters	Print Speed	50 mm/s
	Print Pressure	5 kg
	Separation Distance	2 mm
	Separation Speed	5 mm/s
Pick-and-Placement	Panasonic NPM-WX	
Reflow	Pyramax™ BTU N100	
Inspection	DAGE Quadra 7	

Table 5 summarizes the three trials, each consisting of sixteen experimental combinations. For every combination, three panels were reflowed, yielding thirty-six QFN68 packages per reflow, except in Trial 3 where seventy-two packages were assembled.

- Trial 1: Compared the voiding performance of Pastes 1, 2, and 3 using Profiles A and B with a 4-mil stencil on OSP surface finishes.
- Trial 2: Evaluated the same pastes and profiles with a 4-mil stencil on an ImSn surface finish.
- Trial 3: Assessed the pastes and profiles with a 5-mil stencil on OSP surface finish.

Table 5. Experimental Trials

Trial #	Paste	Reflow Profiles	Stencil Thickness	Component #	Surface Finish
1	Paste 1	A	4	36	OSP
1	Paste 1	B	4	36	OSP
1	Paste 2	A	4	36	OSP
1	Paste 2	B	4	36	OSP
2	Paste 1	A	4	36	ImSn
2	Paste 1	B	4	36	ImSn
2	Paste 2	A	4	36	ImSn
2	Paste 2	B	4	36	ImSn
3	Paste 1	A	5	72	OSP
3	Paste 1	B	5	72	OSP
3	Paste 2	A	5	72	OSP
3	Paste 2	B	5	72	OSP

Voiding Inspection

After reflow, the PCBs were inspected for voids with the DAGE Quadra 7. The voiding data captured was then analyzed with JMP®. For each testing condition, thirty-six assemblies were analyzed for voiding, except in Trial 3, where seventy-two assemblies were built and analyzed. The

increased quantity in Trial 3 was due to the first set of thirty-six assemblies being used to verify results from the second set. The goal was to find the best combination of solder paste, reflow profile, and stencil thickness, and board metallization to achieve an overall average voiding amount below 15%.

RESULTS AND ANALYSIS

Trial 1. The Impact of Profiles Changing Soaking Time to Between 180°C and 220°C with 4 mil Thick Stencil with OSP

In Trial 1, the reflow profile was modified by increasing the ramp rate. The previous slope of 0.64°C/s between 180–200°C was adjusted from profile P4 to 1.0°C/s and 1.5°C/s between 180–220°C for profiles A and B. Our earlier study demonstrated that this ramp rate modification reduced voiding to approximately 12.5%[1]. In the present work, we investigate whether further increasing the ramp rate within this extended temperature window can achieve additional void reduction using the same fluxes evaluated in the prior study, following the observed trend.

Out of thirty-six reflowed assemblies under the modified profiles, Figures 4 and 5 present the one-way ANOVA results for overall voiding and largest void area, respectively, for both profiles using 4 mil OSP surface finish. Among both pastes, the profile modification again had the greatest effect on Paste 2, reducing overall voiding to 11.0% and 9.0% under Profiles A and B, respectively, according to the Tukey Kramer connecting letter report. A similar trend was observed for the largest void area, which was reduced to below 2% for Paste 2 across both profiles according to the Tukey Kramer connecting letter analysis.

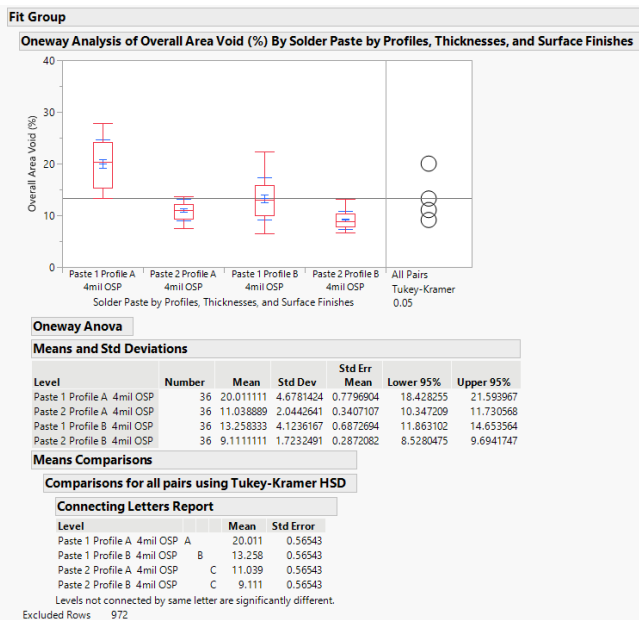


Figure 4. One-way ANOVA Overall Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for Trial 1

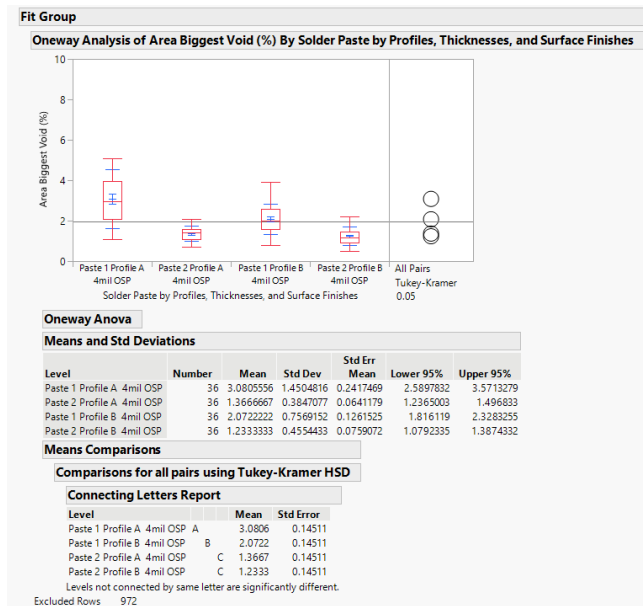


Figure 5. One-way ANOVA Area Biggest Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for Trial 1

Trial 2. Impact of Reflow Profiles on ImSn Surface Finish with 4 mil Stencil Thickness.

Only a slight reduction in voiding was observed with OSP in Trial 1 going from profile A to B for Paste 2. These results differ from the previous study, where the lowest voiding was achieved with Paste 2 at 12.5% with profile P4, whereas the other profiles tested produced significantly higher voiding percentages[1]. Trial 2 was conducted to evaluate whether changing the surface finish to ImSn would have a greater impact. Although the surface finish was changed, the effect of profile modification followed a similar trend to that observed in Trial 1, but with overall higher voiding percentages.

Out of thirty-six reflowed assemblies under the modified profiles, Figures 6 and 7 present the one-way ANOVA results for overall voiding and largest void area, respectively, for both profiles using a 4 mil ImSn surface finish. Among the two pastes, the profile modification again had the greatest effect on Paste 2, reducing overall voiding to 14.3% and 13.1% under Profiles A and B, respectively. A similar trend was observed for the largest void area, which was reduced to below 2% for Paste 2 across both profiles. Both data analysis was interpreted from the Tukey Kramer connecting letter report.

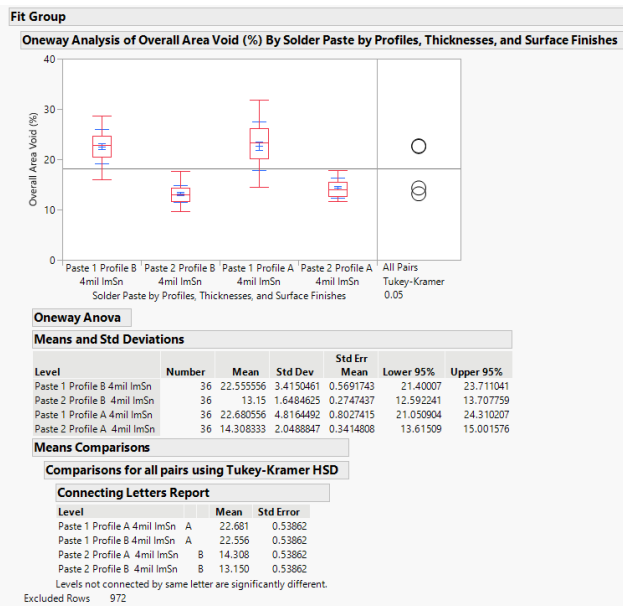


Figure 6. One-way ANOVA Overall Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for Trial 2

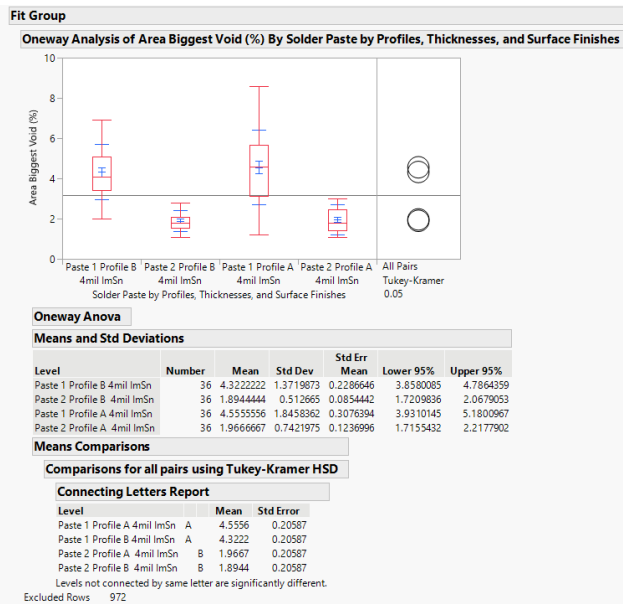


Figure 7. One-way ANOVA Area Biggest Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for Trial 2

Trial 3. Impact of Reflow Profiles on OSP Surface Finish with 5 mil Stencil Thickness

Trial 3 evaluated the impact of reflow profiles on OSP surface finish with a 5-mil stencil thickness. A total of 72 assemblies were reflowed. Overall voiding was consistently lower than in Trials 1 and 2, confirming the benefit of increased stencil thickness. Once again, Paste 2 demonstrated the greatest reduction, with voiding performance of 6.94% and 6.88% under Profiles A and B, respectively. A similar

trend was observed for the largest void area, which was reduced to below 1.5% for Paste 2 across both profiles.

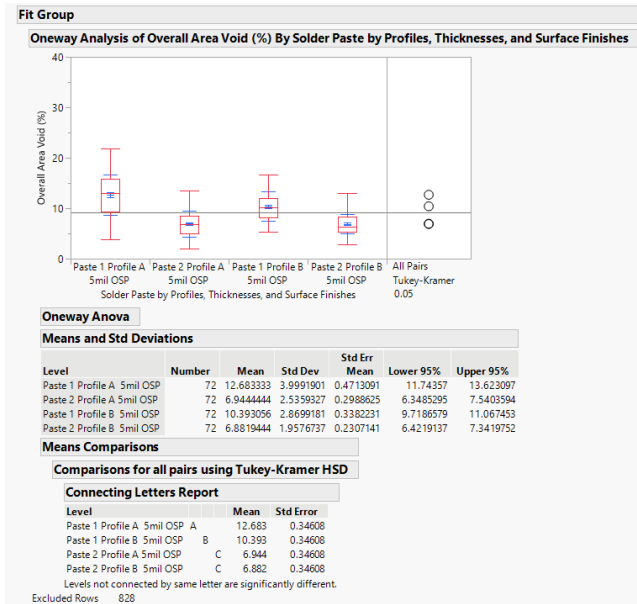


Figure 8. One-way ANOVA Overall Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for Trial 3

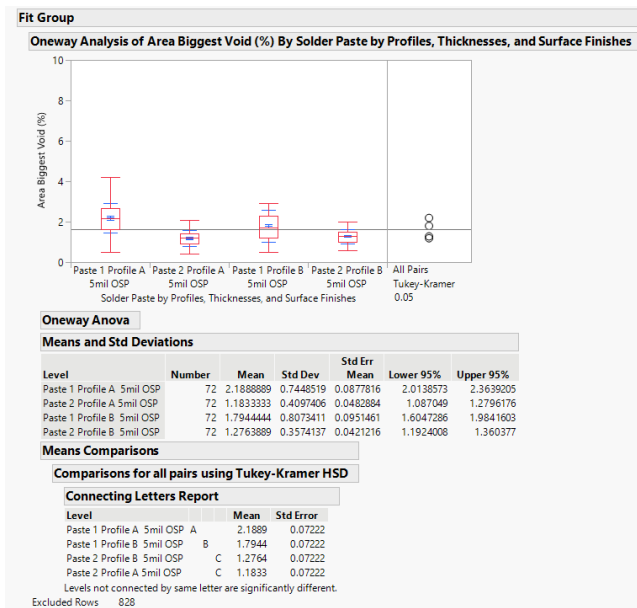


Figure 9. One-way ANOVA Area Biggest Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for Trial 3

Across the three trials, a clear progression in voiding performance was observed, shaped by the combined effects of surface finish, stencil thickness, alloy, and profile, as shown in the one-way ANOVA overall voiding and largest void area analyses in Figures 10 and 11. Trial 1 (OSP, 4 mil) showed only a modest impact from reflow profile modification, with overall voiding for Paste 2 reduced to 11% and 9.0%. Trial 2 (ImSn, 4 mil) followed

a similar profile-driven trend but with consistently higher voiding performance, with Paste 2 reduced to 14.3% and 13.1%. The higher voiding observed with ImSn underscores the importance of surface finish, particularly in combination with SAC305, which exhibited the worst performance in this study.

In contrast, the mixed-alloy system (Paste 2) consistently achieved lower voiding across both OSP and ImSn conditions, reinforcing alloy selection as a secondary but important lever. Trial 3 (OSP, 5 mil) demonstrated the lowest voiding overall, with Paste 2 achieving values of 6.94% and 6.88%, well below the IPC-A-610 Class 3 threshold. This confirms the strong influence of stencil thickness in reducing voiding, while also highlighting that alloy performance interacts with surface finish. The mixed-alloy solder paste paired with OSP and a 5-mil stencil delivered the most robust voiding IPC compliance and lowest overall risk.

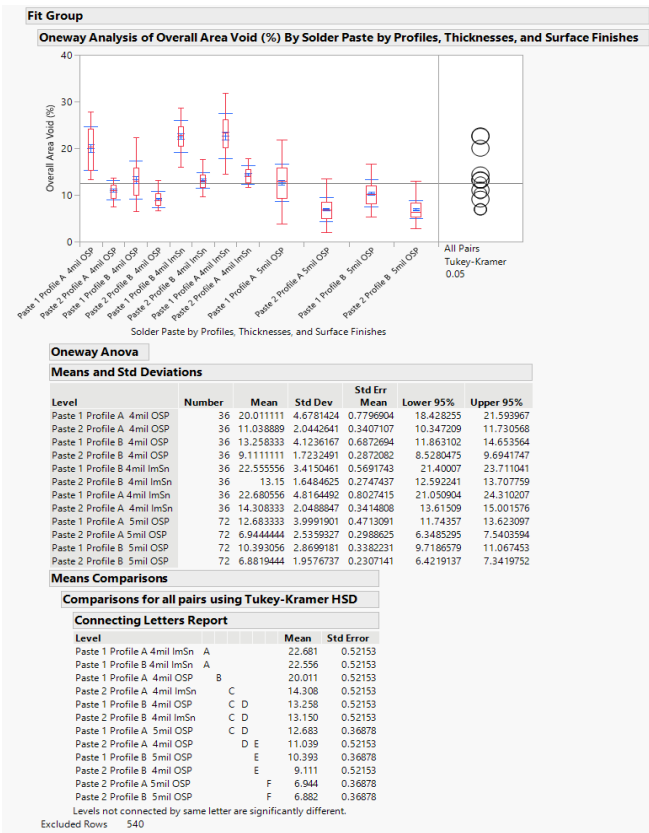


Figure 10. One-way ANOVA Overall Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for all Trials

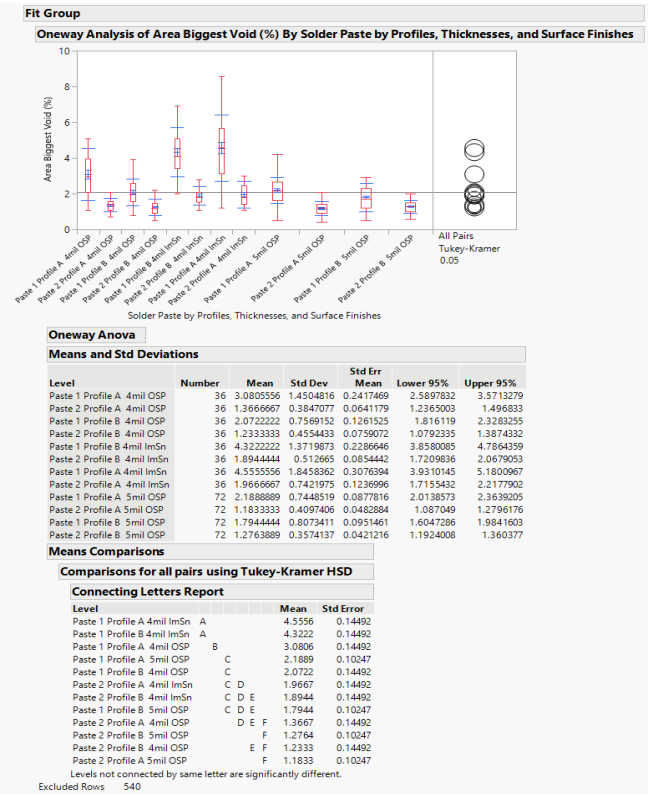


Figure 11. One-way ANOVA Area Biggest Void Data Analysis and Tukey-Kramer Comparison for Jabil Boards with QFN Components for all Trials

DISCUSSION

Summary of Factor Importance and Predicted Trends

The statistical analysis presented in Figure 12 confirms that stencil thickness is the most influential factor affecting solder joint voiding in QFN assemblies. Assemblies printed with the 5-mil stencil consistently exhibited lower voiding compared to those printed with the 4-mil stencil. This trend held across all solder pastes and reflow profiles. The effect is attributed to increased solder volume, which creates a deeper molten pool during reflow. This facilitates more effective outgassing of volatiles, resulting in reduced void formation.

Solder paste composition was the next most significant contributor. Paste 2, a mixed-alloy DFHR material, outperformed the SAC305 control (Paste 1) across all test conditions. Its enhanced wetting behavior and early coalescence likely allow for more efficient volatile release, leading to fewer and smaller voids.

Reflow profile was the third key factor. Profile B, characterized by a slightly faster ramp rate between 180°C and 220°C, consistently reduced voiding relative to Profile A. This profile likely promotes earlier flux activation and more efficient outgassing during the critical reflow phase. However, the impact of reflow profile, while measurable, was secondary to stencil thickness and solder paste selection.

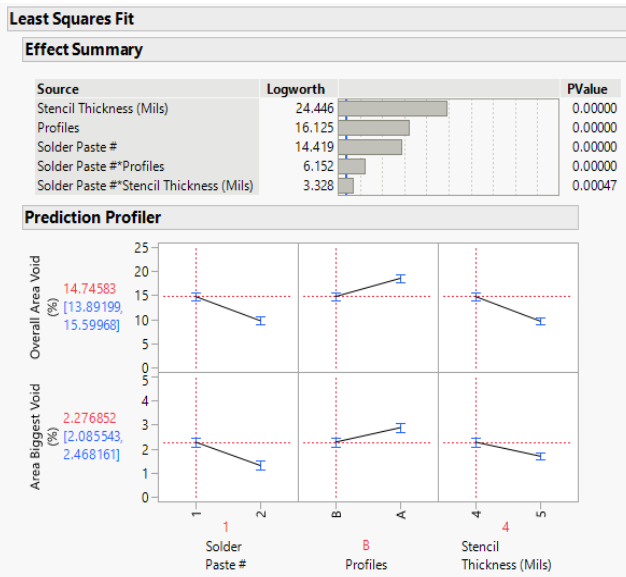


Figure 12. Effect Summary and Prediction Profiler of Multiple Factors

Figures 13 and 14 reinforce this hierarchy. In Figure 13, which displays the main effects for percent voiding, the slope for stencil thickness is the steepest, visually confirming its dominant role. Paste and profile also exhibit clear trends, but with smaller effect sizes. Figure 14, showing the largest individual voids, reveals a similar pattern. The highest single-void sizes occurred with the 4-mil stencil and Paste 1 under Profile A, while the smallest voids were observed using the 5-mil stencil, Paste 2, and Profile B.

Interaction effects were also statistically significant, particularly between Paste $\times$ Profile and Paste $\times$ Stencil Thickness. These interactions demonstrate that the benefits of Profile B and thicker stencils are not uniform across all materials. For example, the advantages of Profile B were most pronounced when paired with Paste 2. Additionally, the performance gap between pastes widened under the 4-mil stencil condition, suggesting that material-process compatibility is critical when solder volume is limited.

Taken together, these results establish a clear hierarchy of influence:

Stencil Thickness $\gg$ Reflow Profile $>$ Solder Paste $>$ Paste $\times$ Profile $>$ Paste $\times$ Stencil Thickness

Interactions between solder paste and stencil thickness, while statistically significant, were the smallest in magnitude.

This analysis supports a key interpretation: stencil thickness sets the baseline for void performance, while reflow profile and solder paste offer opportunities for further optimization. Importantly, reflow adjustments alone cannot overcome limitations imposed by stencil design or suboptimal material choices.

Finally, these results align with the reduced-factor design of experiment (DOE) approach used in this study. The decision to focus on OSP surface finish helped isolate and evaluate the primary process variables without introducing confounding effects. Future work will expand this analysis to include ImSn surface finishes to confirm whether these findings generalize to other production-relevant surface metallization.

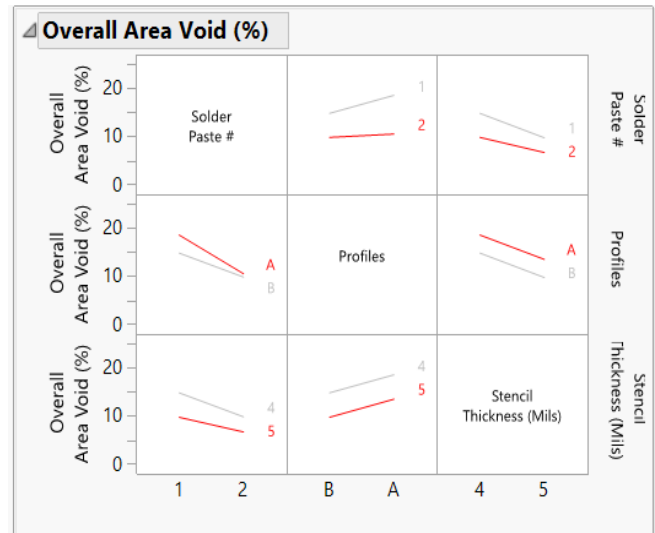


Figure 13. Interaction Profiles of Overall Area Void %

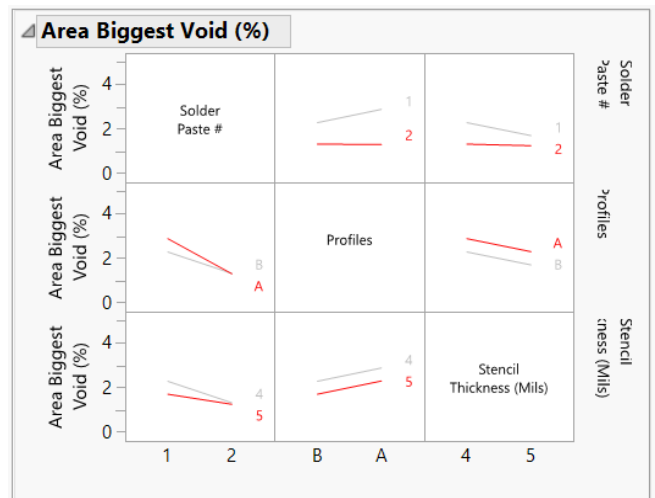


Figure 14. Interaction Profiles of Area Biggest Void %

Figure 15 presents representative X-ray images of QFN components assembled using an OSP surface finish. The comparison includes two solder pastes (Paste 1 and Paste 2), two stencil thicknesses (4 mil and 5 mil), and two reflow profiles (Profile A and Profile B).

Clear differences in voiding behavior were observed. Assemblies produced with the 4-mil stencil showed a higher percentage of voiding compared to those made with the 5-mil stencil. This is likely due to thinner solder deposits restricting the release of entrapped gases during reflow.

Paste 2 generally exhibited smaller and more evenly distributed voids than SAC305, especially when used with the 5-mil stencil. These observations suggest that reflow profiles influence not only the overall voiding level but also the shape and distribution of the voids.

Since void morphology can impact both thermal performance and mechanical reliability, future studies should investigate how void distribution correlates with long-term reliability. This includes further testing under thermal cycling and mechanical stress conditions.

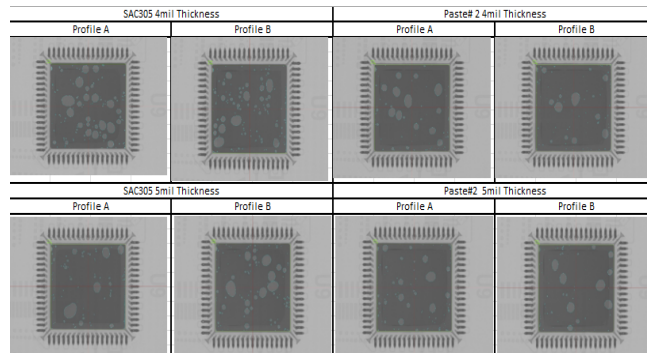


Figure 15. Representative of X-ray Images of OSP 4-mil and 5-mil Stencil

CONCLUSION

This study demonstrates that solder joint voiding in QFN assemblies is primarily influenced by material-related factors. Among these, stencil thickness emerged as the dominant variable, with the 5-mil stencil consistently producing lower voiding levels compared to the 4-mil stencil. Adjustments to the reflow profile had a measurable but secondary effect on voiding, while the choice of solder paste contributed to a lesser effect.

These findings highlight that selecting favorable material combinations is critical to achieving voiding performance targets and ensuring process compliance. It should be noted that ImSn surface finish data could not be included in this analysis due to limited data availability, as Trial 3 focused primarily on OSP finishes.

These results underscore the importance of optimizing material selection early in the process development phase, as this provides a more robust foundation for subsequent fine-tuning of process parameters such as reflow profiles. For BTCs, voiding acceptance criteria beyond IPC-A-610 are often defined as “as agreed between user and supplier” (AABUS).

Overall, compliance to IPC-A-610 Class 3 requirements was reliably achieved only under favorable material combinations, most notably OSP with 5 mil stencils and the mixed-alloy solder paste. These findings highlight that stencil thickness, profile, and solder paste choice are the critical levers for voiding reduction. It is especially relevant to

automotive and aerospace electronics, where voiding control is essential.

In the previous study, reflow profile modification was identified as a major factor in reducing voiding[1]. In that work, profiles were evaluated within a single and mixed alloy solder paste/stencil thickness system. In the present broader DOE, profile changes continued to show a measurable effect, but the impact was secondary compared to stencil thickness. This indicates that while profile optimization can reduce voiding within a given material set, material-driven factors ultimately dominate voiding behavior across assemblies.

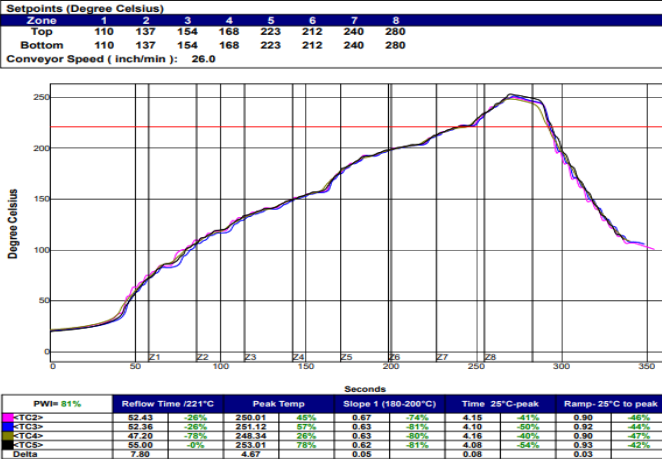
Future work will extend this methodology to include additional surface finishes (e.g., ImSn, ENIG, ENEPIG), expanded stencil architecture, cross-sectional analysis, and mechanical reliability testing to correlate voiding performance with long-term thermal cycling results. Profiles producing smaller, dispersed voids are expected to offer better long-term reliability. This highlights that not only the quantity but also the morphology of voiding is an important reliability factor, warranting further investigation in future work.

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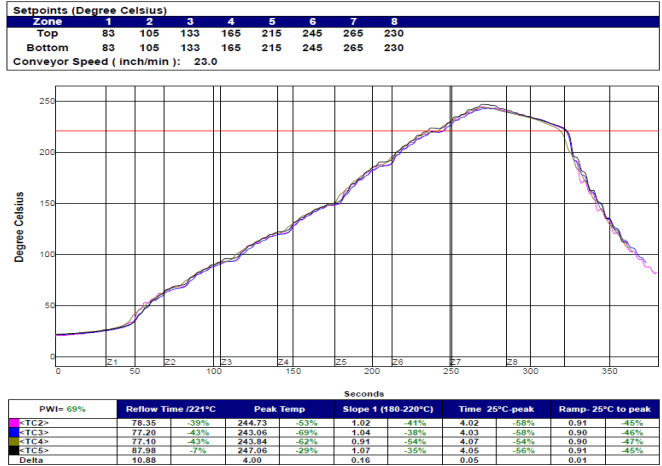
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APPENDIX
Profile P4



Profile A



Profile B

