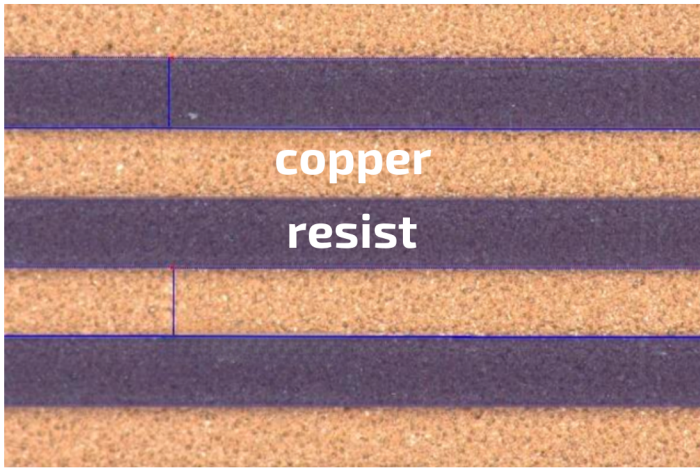
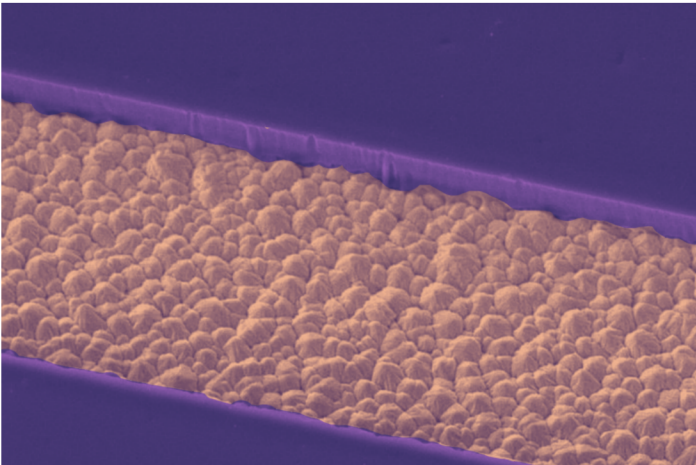


# SEM Inner-Layer after Develop Unetched

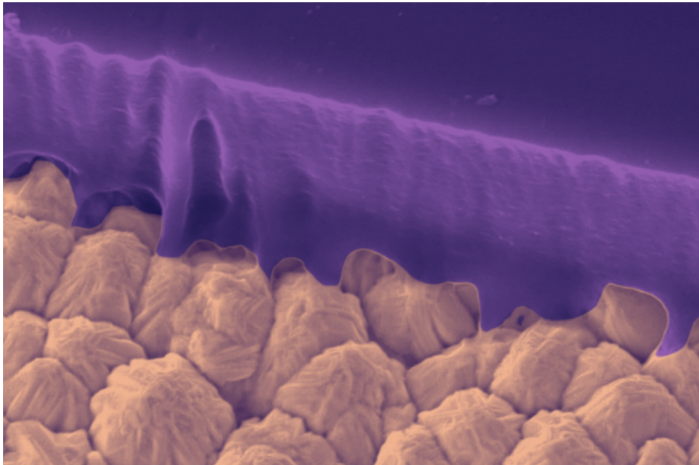
Scanning Electron Microscopy photos of what an imaged feature may look like at the photoresist level (colorized).



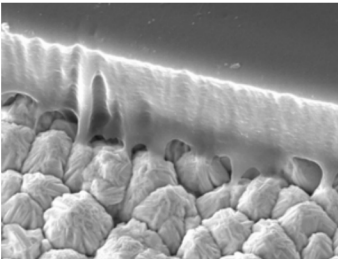
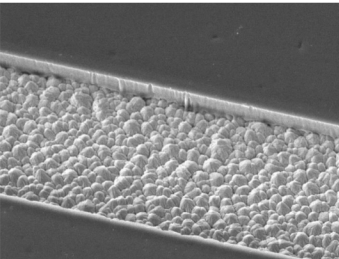
1x



1000x



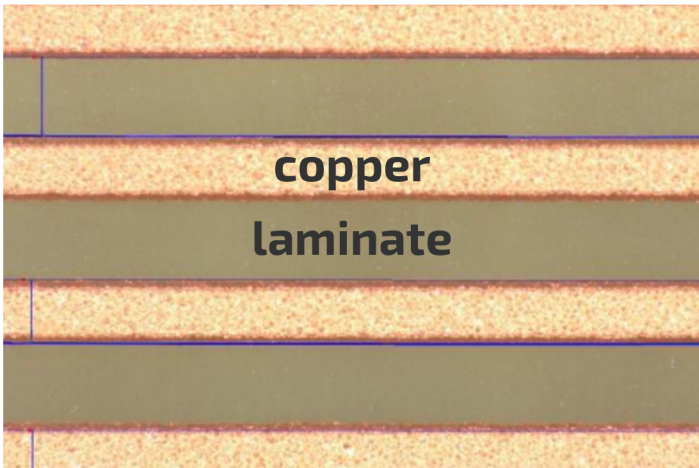
3000x



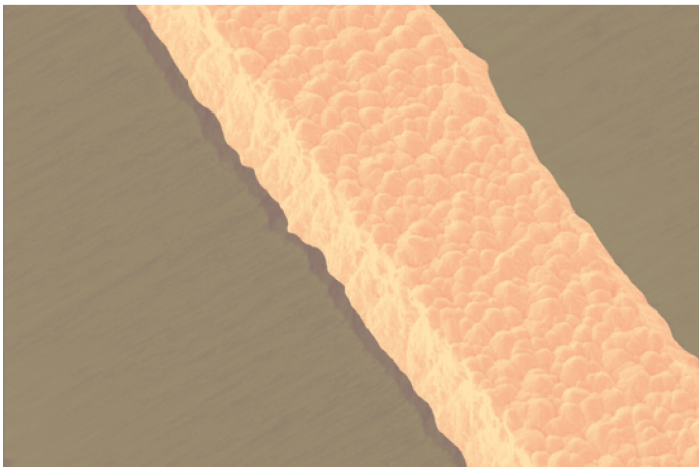
American Standard Circuits  
Sunstone Circuits

# SEM Inner-Layer Etched

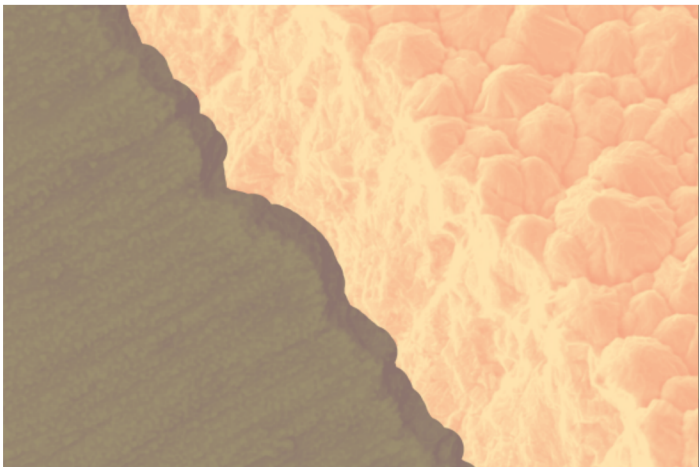
Scanning Electron Microscopy photos of what an imaged feature may look like at the etched level (colorized).



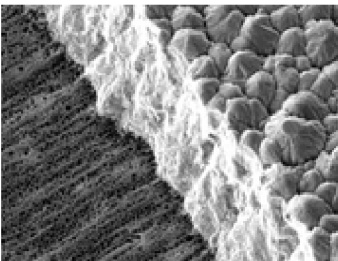
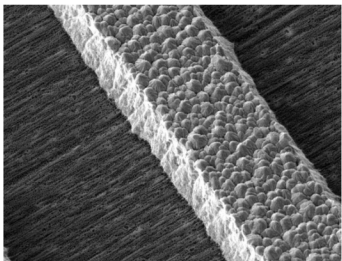
1x



1000x



3000x

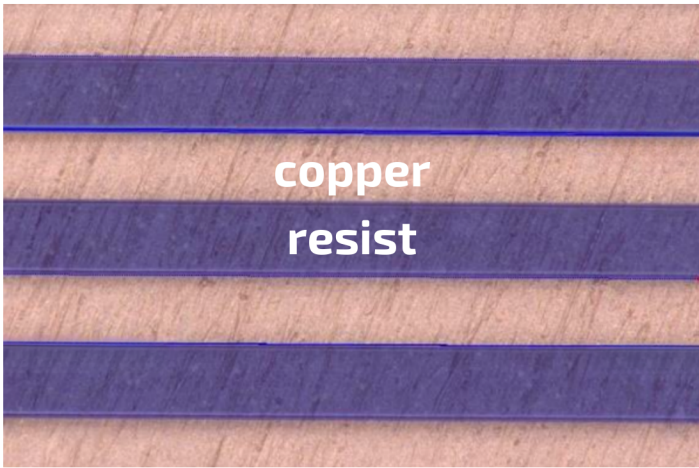


American Standard Circuits  
Sunstone Circuits

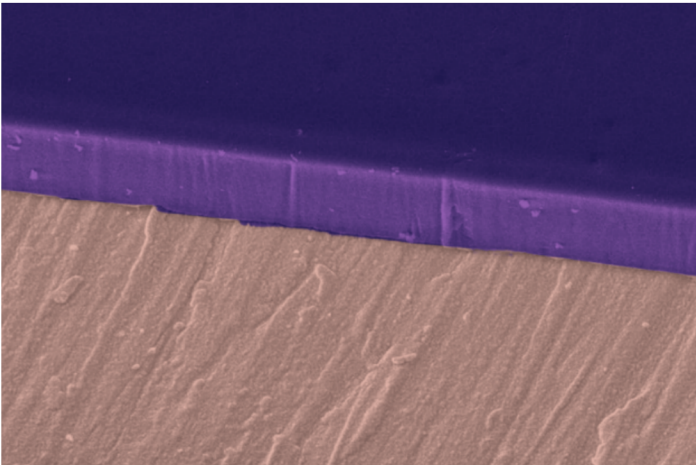


# SEM Outer-Layer after Develop Unetched / Unplated

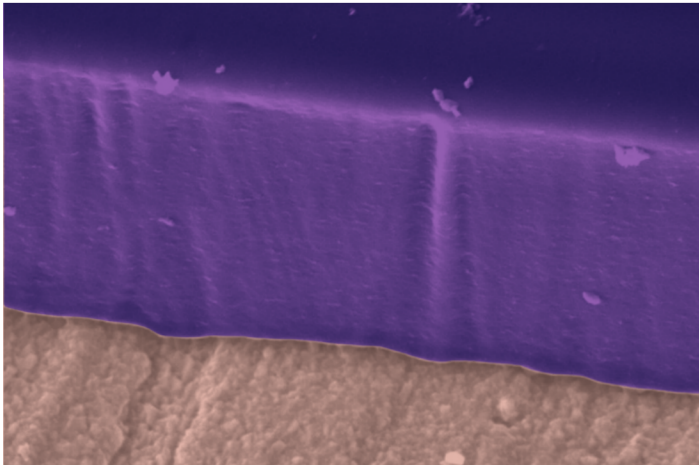
Scanning Electron Microscopy photos of what an imaged feature may look like at the photoresist level (colorized).



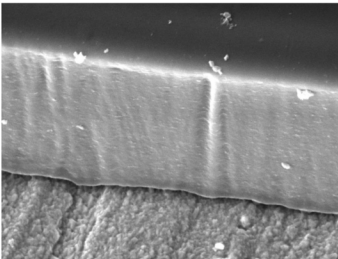
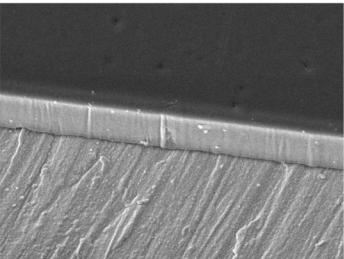
1x



1000x

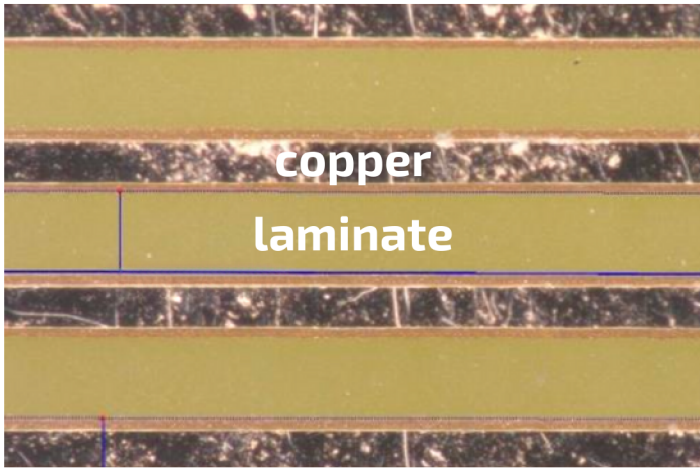


5000x

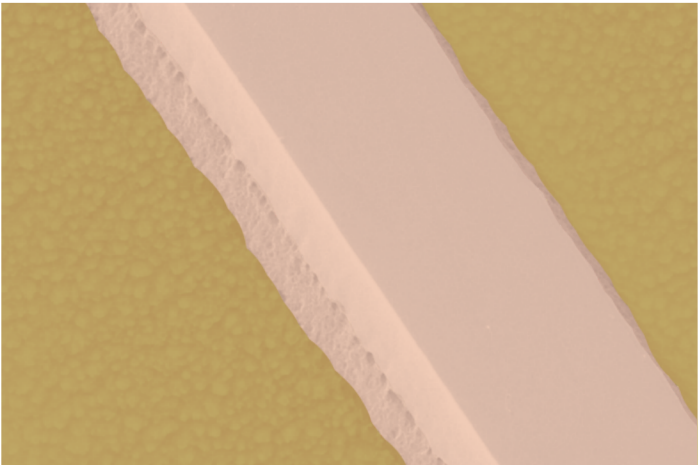


# SEM Outer-Layer Etched

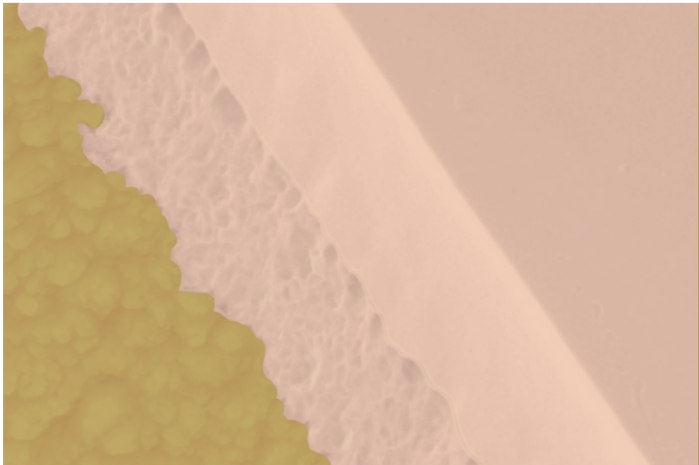
Scanning Electron Microscopy photos of what an imaged feature may look like at the etched level (colorized).



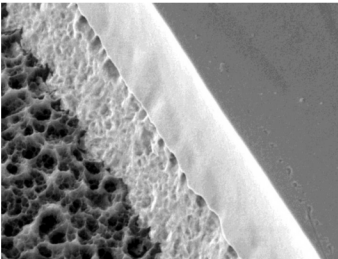
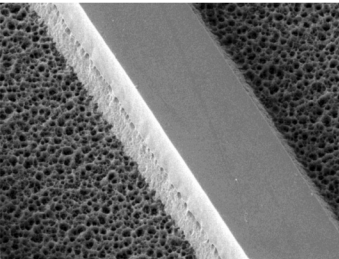
1x



1000x



3000x



American Standard Circuits  
Sunstone Circuits